3501
1024-BIT STATIC READ-ONLY MEMORY
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3501 is a 1024-bit read-only memory in a 128 word by 8 bit format. It is a MOS monolithic integrated circuit utilizing P-channel enhancement mode technology. The fixed program memory must be specified by the customer and is customized by modifying one mask in the fabrication process. This results in a fast turn-around, low cost custom memory.

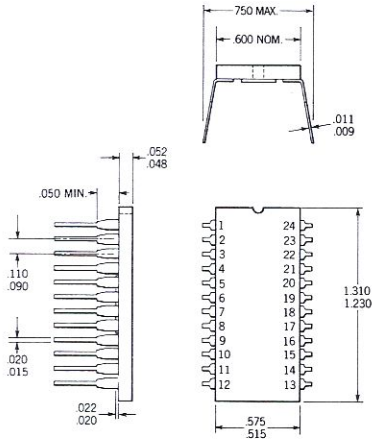
FEATURES:
- **CHIP SELECT**
- **ACCESS TIME — 2.5 μs TYP.**
- **STATIC OPERATION**
- **LOW POWER CONSUMPTION — 120 mW TYP.**
- **BIPOLAR COMPATIBLE OUTPUTS**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

All Voltages and Data Input Lines	−30 V to +0.3 V
Power Dissipation	250 mW
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C
	0°C to +70°C

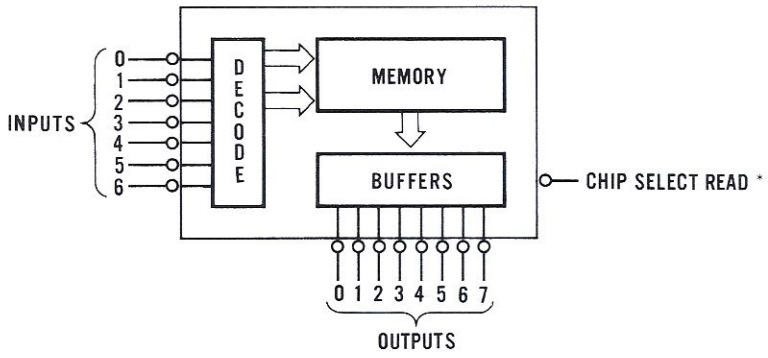
APPLICATIONS:
- Micro Programming
- Code Conversion
- Table Lookup
- Control Logic

PHYSICAL DIMENSION



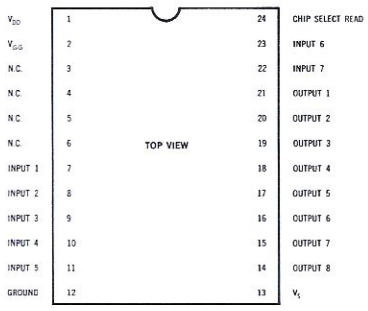
ORDER PART NO. A6G3501X4X (−55°C to +85°C)
A6G3501X9X (0°C to +70°C)

LOGIC DIAGRAM (MIL STD 806B)



*WHEN CHIP SELECT READ IS AT GROUND THE OUTPUTS ARE FLOATING.

PIN CONFIGURATION



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

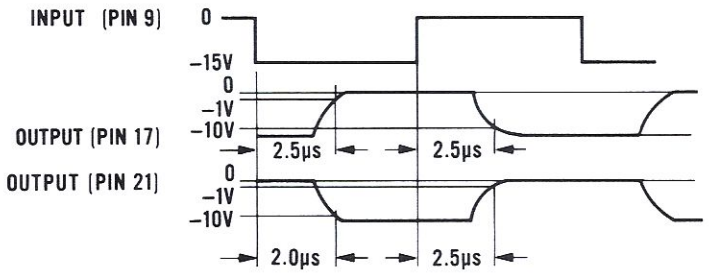
COPYRIGHT FAIRCHILD SEMICONDUCTOR 1968 • PRINTED IN U.S.A. 74-BR-0002-48 35M
MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

FAIRCHILD MOS INTEGRATED CIRCUIT 3501

ELECTRICAL CHARACTERISTICS Standard Conditions (unless otherwise specified)
$V_{DD} = -13\ V \pm 1\ V$, $V_{GG} = -27\ V \pm 2\ V$, $V_S = -27\ V \pm 2\ V$
Load 10 MΩ, 10 pF, $T_A = 25°C$

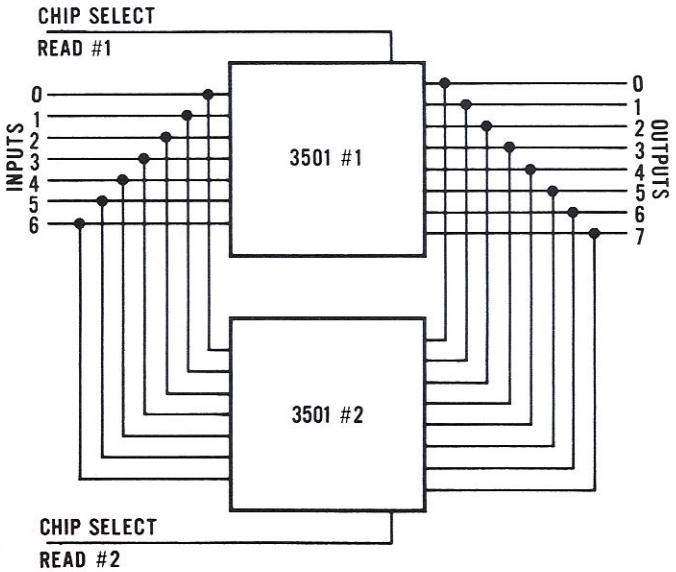
CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Logic Levels					
Logic 0	0		−2.0	Volts	
Logic 1	−9.0			Volts	
Output Pulse Delay		2.5	4.0	μs	
Output Logic Levels					
Logic 0	0		−1.0	Volts	
Logic 1	−10			Volts	
Logic 1	−5.0	−7.0		Volts	$R_L = 4.0\ k\Omega$, $V_S = -15\ V$
Output Capacitance		5.0		pF	
Input Capacitance		7.0		pF	
Input Leakage			5.0	μA	$V_{IN} = -20\ V$
Supply Current Drain					
I_{DD}			6.5	mA	
I_{GG}			4.0	mA	
Power Consumption		120		mW	

TIMING DIAGRAM (TYPICAL)



INPUT PINS 7, 8, 10, 11, 22, 23, GROUND
WORST CASE CONDITION INPUT 0 OUTPUT 0

TYPICAL EXPANDED MEMORY



CONNECTION FOR 256 WORDS 8 BITS

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.